Applicant : Michael P. Cornaby et al.
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REMARKS

Claims 1-38 are pending and rejected by the examiner. Claims 1, 8 and 32 are independent claims.

The examiner objected to the abstract.

Applicant has amended the abstract to comply with the requirements of 37 C.F.R. §1.72(b). The abstract, as amended, enables the reader thereof, regardless of his or her degree of familiarity with patent documents, to determine quickly from a cursory inspection of the nature and gist of the technical disclosure and includes that which is new in the art to which the invention pertains. No new matter was added.

The examiner continues to reject claims 1-38 under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, the examiner is not clear as to what is the structure of the stack and what is an "out-of-order" stack.

As is well known to those skilled in programming, an ordinary or typical in-order "stack" is a type of data structure in which items are in the reverse order from that in which they are added, so the most recently added item is the first removed. This is also called "last-in, first-out (LIFO)." Traditionally, program instructions are pushed on to an in-order stack and then popped off in a LIFO manner.

Applicant's claims 1, 8 and 32 include an out-of-order stack. More specifically, applicant's claims include an out-of order microinstruction pointer (μIP) stack. Applicants describe this out-of-order stack in their detailed description (and in a previous response to the examiner). To reiterate, microinstruction pointers that are stored in the out-of-order μIP stack are aggressively re-ordered to allow them to execute as quickly as their input micro-operands are ready. This out-of-order execution allows microinstructions in the microprogram following

delayed microinstructions to proceed around them as long as they do not depend on those delayed microinstructions.

Applicants' claim 2 introduces a retirement indicator field. This field is used to reorder the microinstruction pointers, executed in an out-of-order manner, back to an original microprogram order.

As stated in an earlier response, microcode executes in the micro core and performs microoperations, while microinstructions are used to manipulate the microinstruction pointer stack.

Accordingly, claims 1-38 are proper under 35 U.S.C. §112, second paragraph, and the examiner rejection should be withdrawn.

The examiner uses Gage to reject claims 1, 3, 4, 8, 10, 11, 15-22 and 26-38 as having been anticipated.

Claims 1, 8 and 32 include an out-of-order microinstruction pointer (μIP) stack. Gage neither describes nor suggest an out-of-order microinstruction pointer (μIP) stack. On the contrary, Gage discloses a typical in-order stack that is circular, i.e., if the number of calls to the stack exceeds the number of entries in the stack (i.e., as the calls progress through the stack in an in-order fashion), the first call to exceed the number of entries in the stack causes an address to be placed back on the top of the stack, overwriting the original address that was position on the top of the stack. All this occur successively and in-order. Accordingly, claims 1, 8 and 32 are not anticipated by Gage.

It is believed that all of the pending claims have been addressed. However, the absence

of a reply to a specific rejection, issue or comment does not signify agreement with or

concession of that rejection, issue or comment. In addition, because the arguments made above

may not be exhaustive, there may be reasons for patentability of any or all pending claims (or

other claims) that have not been expressed. Finally, nothing in this paper should be construed as

an intent to concede any issue with regard to any claim, except as specifically stated in this

paper, and the amendment of any claim does not necessarily signify concession of

unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: January 3, 2005

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